## WHAT IS CLAIMED IS:

1		1.	1.	An integrated circuit chip comprising:			
2		a subs	trate, the	e substrates comprising a plurality of chip structures;			
3	a plurality of bonding pads disposed on the substrate, each of the bonding pads						
4	being formed	being formed from an aluminum bearing material;					
5		a surface region formed on each of the bonding pads;					
6		an under bump metal layer overlying the surface region;					
7		a wetting layer formed overlying the surface region, the wetting layer					
8	comprising a	orising a plurality of protrusions extending out of the wetting layer and disposed spatially					
9	on the wetting	e wetting layer;					
10		a bump layer overlying the wetting layer and mechanically coupling the					
11	plurality of protrusions.						
1		2.	The ch	nip of claim 1 wherein the under bump metal comprises an			
2	adhesive material, a wetting material, and a protective material.						
-		, , , , , , , , , , , , , , , , , , ,	vouing .	material, and a proceeding material.			
1		3.	The ch	ip of claim 1 wherein each of the protrusions has a			
2	predetermined	etermined height and a predtermined width.					
1		4.	The ch	nip of claim 1 wherein each of the protrusions has a			
2	predetermine			ight ranging from about 15 to about 20 microns.			
	1	J	•				
1		5.		nip of claim 1 wherein each of the bonding pads has a dimension			
2	of about 80 microns by about 80 microns.						
1		6.	The ch	nip of claim 1 wherein the wetting layer is provided by a			
2	deposition or						
	1		•				
1		7.	The ch	nip of claim 1 wherein the plurality of protrusions prevents a			
2	possibility of	possibility of the bump layer from peeling from the surface region of the bonding pad.					
1		8.	The ch	nip of claim 1 wherein the plurality of protrusions prevents a			
2	possibility of	possibility of the bump layer from peeling from the surface region during a reflow process.					
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1		9	The ch	nip of claim 1 wherein the substrate comprises silicon			

1		10.	The chip of claim 1 wherein the substrate is a silicon on insulator				
2	wafer.						
1		11.	A method for fabricating an integrated circuit chip comprising:				
2		providing a substrate;					
3		forming a plurality of bonding pads overlying the substrate, each of the					
4	bonding pads	ing pads being formed from an aluminum bearing material and including a surface					
5	region;						
6		forming an under bump metal layer overlying the surface region;					
7		forming a wetting layer overlying the under bump metal layer, the wetting					
8	layer comprising a plurality of protrusions extending out of the wetting layer and disposed						
9	spatially on the wetting layer; and						
10		forming a bump layer overlying the wetting layer and mechanically coupling					
11	to the plurality of protrusions.						
1		12.	The method of claim 11 wherein the under bump metrology comprises				
2	an adhesive material, a wetting material, and a protective material.						
1		13.	The method of claim 11 wherein each of the protrusions has a				
2	predetermined	ined height and a predtermined width.					
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1		14.	The method of claim 11 wherein each of the protrusions has a				
2	predetermined height, the height ranging from about 15 to about 20 microns.						
1		15.	The method of claim 11 wherein each of the bonding pads has a				
2	dimension of about 80 microns by about 80 microns.						
_	difficusion of	ubbut b	o microns by about 60 microns.				
1		16.	The method of claim 11 wherein the wetting layer is provided by a				
2	deposition or plating process.						
1		17.	The method of claim 11 wherein the plurality of protrusions prevents a				
2	possibility of the bump layer from peeling from the surface region of the bonding pad.						
1		18.	The method of claim 11 further comprising reflowing the bump layer				
2	while maintai		e bump layer on the surface region through the plurality of protrusions.				
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